We claim:

1. A method of removing a high k dielectric layer from a substrate comprising the steps of:

(a) providing a substrate with a high k dielectric layer formed thereon;

(b) depositing a gate layer and forming a gate electrode on said high k dielectric layer that exposes portions of said high k dielectric layer; and

(c) etching through said exposed portions of said high k dielectric layer with a plasma etch comprised of an inert gas, BCl_3, and one or more fluorocarbon gases or CH_4.

2. The method of claim **1** wherein said plasma etch is further comprised of a low bias power of about 10 to 50 Watts.

3. The method of claim **1** wherein said high gate dielectric layer is formed by a chemical vapor deposition (CVD), metal organic CVD (MOCVD), or an atomic layer deposition (ALD) process and has a thickness between about 15 and 100 Angstroms.

4. The method of claim **1** wherein said high k dielectric layer is comprised of one or more of HfO_2, ZrO_2, Ta_2O_5, TiO_2, Al_2O_3, Y_2O_3 or La_2O_5.

5. The method of claim **1** wherein said high k dielectric layer is a silicate, aluminate, nitride, or oxynitride of Hf, Zr, Ta, Ti, Y, or La.

6. The method of claim **1** wherein the high k dielectric layer is subjected to a post-deposition surface treatment or an anneal step prior to forming a gate layer on said high k dielectric layer.

7. The method of claim **6** wherein said anneal step is comprised of heating the substrate in an O_2 or H_2 ambient at about $800^{o}C$ for a period of about 20 minutes.

8. The method of claim **1** wherein said gate layer is comprised of polysilicon, amorphous silicon, Si-Ge, W, Ta, Al, Ti, Ni, Ru, Pa, Pt, Mo, TiN, TaN, or TaSiN.

9. The method of claim **1** wherein said gate layer has a thickness between about 500 and 1500 Angstroms.

10. The method of claim **1** wherein said plasma etch is performed with BCl_3, an inert gas comprised of Ar, He, Ne, or Xe, and one or more fluorocarbon gases $C_XH_YF_Z$ where x and z are integers and y is an integer or is 0 including CF_4, CHF_3, CH_2F_2, CH_3F, C_2HF_5, $C_2H_2F_4$, and C_2F_6.

11. The method of claim **1** wherein said plasma etch is performed with a BCl_3 flow rate of about 100 to 400 standard cubic centimeters per minute (sccm), a fluorocarbon gas flow rate from about 5 to 20 sccm, and an inert gas flow rate between about 100 and 500 sccm.

12. The method of claim **1** wherein said plasma etch is performed with a chamber pressure from about 5 to 20 mTorr and a substrate temperature between about 50°C and 70°C.

13. The method of claim **1** wherein said plasma etch is performed with a RF power between about 200 and 800 Watts.

14. The method of claim **1** wherein said plasma etch is continued until an end point is reached as indicated by a drop in an OES signal for a metal in the high k dielectric layer or is carried out for a period of about 60 to 90 seconds.

15. The method of claim **1** further comprised of forming an interfacial layer that is SiO_2, silicon nitride, or silicon oxynitride on said substrate prior to forming said high k dielectric layer.

16. The method of claim **15** wherein said interfacial layer is removed during the same plasma etch step that removes the high k dielectric layer.

17. The method of claim **1** wherein said high k dielectric layer is etched at a rate that is more than about ten times the etch rate of said gate electrode under the same conditions.

18. The method of claim **1** further comprised of a wet clean step after the plasma etch through the high k dielectric layer is complete.

19. The method of claim **1** further comprised of forming a spacer on opposite sides of said gate electrode before etching through said high k dielectric layer.

20. A method of forming a MOSFET, comprising:

(a) providing a substrate having shallow trench isolation features which separate active regions:

(b) forming a high k dielectric layer on said substrate;

(c) depositing a gate layer on said high k dielectric layer and etching through said gate layer to form a gate electrode and expose portions of said high k dielectric layer, said gate electrode is aligned over an active region; and

(d) etching through exposed portions of said high k dielectric layer with a plasma etch comprised of an inert gas, BCl_3, and one or more fluorocarbon gases or CH_4.

21. The method of claim **20** wherein step (d) is further comprised of a low bias power of about 10 to 50 Watts.

22. The method of claim **20** wherein said high k dielectric layer is formed by a CVD, MOCVD, or ALD process and has a thickness between about 15 and 100 Angstroms.

23. The method of claim **20** wherein said high k dielectric layer is comprised of one or more of HfO_2, ZrO_2, Ta_2O_5, TiO_2, Al_2O_3, Y_2O_3 or La_2O_5.

24. The method of claim **20** wherein said high k dielectric layer is a silicate, aluminate, nitride, or oxynitride of Hf, Zr, Ta, Ti, Y, or La.

25. The method of claim **20** wherein the high k dielectric layer is subjected to a post-deposition surface treatment or an anneal step prior to forming a gate layer on said high k dielectric layer.

26. The method of claim **25** wherein said anneal step is comprised of heating the substrate in an O_2 or H_2 ambient at about 800^{o}C for a period of about 20 minutes.

27. The method of claim **20** wherein said gate layer is comprised of polysilicon, amorphous silicon, Si-Ge, W, Ta, Al, Ti, Ni, Ru, Pa, Pt, Mo, TiN, TaN, or TaSiN.

28. The method of claim **20** wherein said gate layer has a thickness between about 500 and 1500 Angstroms.

29. The method of claim **20** wherein said etching through exposed portions of said high k dielectric layer is performed with BCl_3, an inert gas comprised of Ar, He, Ne, or Xe, and one or more $C_XH_YF_Z$ gases where x and z are integers and y is an integer or is 0 including CF_4, CHF_3, CH_2F_2, CH_3F, C_2HF_5, $C_2H_2F_4$, and C_2F_6.

30. The method of claim **20** wherein said etching through exposed portions of said high k dielectric layer is performed with a BCl_3 flow rate of about 100 to 400 sccm, a fluorocarbon gas flow rate from about 5 to 20 sccm, and an inert gas flow rate between about 100 and 500 sccm.

31. The method of claim **20** wherein said etching through exposed portions of said high k dielectric layer is performed with a chamber pressure from about 5 to 20 mTorr and a substrate temperature between about 50°C and 70°C.

32. The method of claim **20** wherein said etching through exposed portions of said high k dielectric layer is performed with a RF power between about 200 and 800 Watts.

33. The method of claim **20** wherein said etching through exposed portions of said high k dielectric layer is continued until an end point is reached as indicated by a drop in an OES signal for a metal in the high k dielectric layer or is carried out for a period of about 60 to 90 seconds.

34. The method of claim **20** further comprised of forming an interfacial layer comprised of silicon nitride, SiO_2, or silicon oxynitride on said substrate prior to forming said high k dielectric layer.

35. The method of claim **34** wherein said interfacial layer is removed by the same plasma etch that etches through exposed portions of said high k dielectric layer.

36. The method of claim **20** wherein etching through exposed portions of said high k dielectric layer is performed in the same etch chamber as etching through the gate layer.

37. The method of claim **20** wherein said etching through exposed portions of said high k dielectric layer is performed at a rate that is more than about ten times the etch rate of said gate electrode under the same conditions.

38. The method of claim **20** further comprised of a wet clean step after etching through exposed portions of said high k dielectric layer is complete.

39. The method of claim **20** further comprised of forming a spacer on opposite sides of said gate electrode before etching through exposed portions of said high k dielectric layer.

40. The method of claim **20** further comprised of forming source/drain regions in said substrate and forming a silicide layer on the gate electrode and on source/drain regions in said substrate.